Fornitura di 25 esemplari di 'ITPM Board' per l'elettronica di 'digital processing' dei segnali in radiofrequenza nell'esperimento Aperture Array Verification System 1 (AAVS1).

Allegato 1 – Principali Connessioni da/per FPGA

1. FPGA LOCAL BUS

Banco	Nome Pin	Pin	iTPM segnale FPGA 0	iTPM segnale FPGA 1	iTPM BUS
Bank 65	IO_L7P_T1L_N0_QBC_AD13P_A18	M27	MAN_LB_ACK	MAN_LB_ACK	Local Bus
2v5	IO_L11P_T1U_N8_GC_A10_D26	M25	MAN_LB_AD0	MAN_LB_AD0	Local Bus
	IO_L11N_T1U_N9_GC_A11_D27	M26	MAN_LB_AD1	MAN_LB_AD1	Local Bus
	IO_L10P_T1U_N6_QBC_AD4P_A12_D28	L22	MAN_LB_AD2	MAN_LB_AD2	Local Bus
	IO_L10N_T1U_N7_QBC_AD4N_A13_D29	K23	MAN_LB_AD3	MAN_LB_AD3	Local Bus
	IO_L9P_T1L_N4_AD12P_A14_D30	L25	MAN_LB_AD4	MAN_LB_AD4	Local Bus
	IO_L9N_T1L_N5_AD12N_A15_D31	K25	MAN_LB_AD5	MAN_LB_AD5	Local Bus
	IO_L8P_T1L_N2_AD5P_A16	L23	MAN_LB_AD6	MAN_LB_AD6	Local Bus
	IO_L8N_T1L_N3_AD5N_A17	L24	MAN_LB_AD7	MAN_LB_AD7	Local Bus
	IO_L14P_T2L_N2_GC_A04_D20	P24	MAN_LB_CLK	MAN_LB_CLK	Local Bus
	IO_L3P_T0L_N4_AD15P_A26	K26	MAN_LB_CS0	MAN_LB_CS1	Local Bus
	IO_L7N_T1L_N1_QBC_AD13N_A19	L27	MAN_LB_RESET	MAN_LB_RESET	Local Bus
	IO_L4N_T0U_N7_DBC_AD7N_A25	J25	MAN_RGMII0_ACK	MAN_RGMII1_ACK	Local Bus
	IO_L6P_T0U_N10_AD6P_A20	J23	MAN_RGMII0_CLK	MAN_RGMII1_CLK	Local Bus
	IO_L6N_T0U_N11_AD6N_A21	H24	MAN_RGMII0_D0	MAN_RGMII1_D0	Local Bus
	IO_L5P_T0U_N8_AD14P_A22	J26	MAN_RGMII0_D1	MAN_RGMII1_D1	Local Bus
	IO_L5N_T0U_N9_AD14N_A23	H26	MAN_RGMII0_D2	MAN_RGMII1_D2	Local Bus
	IO_L4P_T0U_N6_DBC_AD7P_A24	J24	MAN_RGMII0_D3	MAN_RGMII1_D3	Local Bus
	IO_T2U_N12_CSI_ADV_B	N27	XIL0_SMAP_CSI	XIL1_SMAP_CSI	SMAP Bus
	IO_L24N_T3U_N11_DOUT_CSO_B	K21	XIL0_SMAP_CSO	XIL1_SMAP_CSO	SMAP Bus
	IO_L22P_T3U_N6_DBC_AD0P_D04	M20	XIL_SMAP_D4	XIL_SMAP_D4	Local Bus
	IO_L22N_T3U_N7_DBC_AD0N_D05	L20	XIL_SMAP_D5	XIL_SMAP_D5	Local Bus
	IO_L21P_T3L_N4_AD8P_D06	R21	XIL_SMAP_D6	XIL_SMAP_D6	Local Bus
	IO_L21N_T3L_N5_AD8N_D07	R22	XIL_SMAP_D7	XIL_SMAP_D7	Local Bus

Table A1-1: FPGA Local bus.

2. JESD B ADC-FPGA

Le line multigigabit di ADC sono connesse nel modo seguente:

Bank	Pin Name	Pin	iTPM signal FPGA 0	iTPM signal FPGA 1
B224	MGTHRXN0	AP1	AD0_SERD0_N	AD8_SERD0_N
	MGTHRXP0	AP2	AD0_SERD0_P	AD8_SERD0_P
	MGTHRXN1	AM1	AD0_SERD1_N	AD8_SERD1_N
	MGTHRXP1	AM2	AD0_SERD1_P	AD8_SERD1_P
	MGTHRXN2	AK1	AD1_SERD0_N	AD9_SERD0_N
	MGTHRXP2	AK2	AD1_SERD0_P	AD9_SERD0_P
	MGTHRXN3	AJ3	AD1_SERD1_N	AD9_SERD1_N
	MGTHRXP3	AJ4	AD1_SERD1_P	AD9_SERD1_P
B225	MGTHRXN0	AH1	AD2_SERD0_N	AD10_SERD0_N
	MGTHRXP0	AH2	AD2_SERD0_P	AD10_SERD0_P
	MGTHRXN1	AF1	AD2_SERD1_N	AD10_SERD1_N
	MGTHRXP1	AF2	AD2_SERD1_P	AD10_SERD1_P
	MGTHRXN2	AD1	AD3_SERD0_N	AD11_SERD0_N
	MGTHRXP2	AD2	AD3_SERD0_P	AD11_SERD0_P
	MGTHRXN3	AB1	AD3_SERD1_N	AD11_SERD1_N
	MGTHRXP3	AB2	AD3_SERD1_P	AD11_SERD1_P
	MGTREFCLK1N	Y5	CLK_JESD_FPGA0_N	CLK_JESD_FPGA1_N
	MGTREFCLK1P	Y6	CLK_JESD_FPGA0_P	CLK_JESD_FPGA1_P
	MGTAVTTRCAL_R	AP6	MGT_AVTT	MGT_AVTT
	MGTRREF_R	AP5	MGTRREF_FPGA0	MGTRREF_FPGA1
B226	MGTHRXN0	Y1	AD4_SERD0_N	AD12_SERD0_N
	MGTHRXP0	Y2	AD4_SERD0_P	AD12_SERD0_P
	MGTHRXN1	V1	AD4_SERD1_N	AD12_SERD1_N
	MGTHRXP1	V2	AD4_SERD1_P	AD12_SERD1_P
	MGTHRXN2	T1	AD5_SERD0_N	AD13_SERD0_N
	MGTHRXP2	T2	AD5_SERD0_P	AD13_SERD0_P
	MGTHRXN3	P1	AD5_SERD1_N	AD13_SERD1_N
	MGTHRXP3	P2	AD5_SERD1_P	AD13_SERD1_P
B227	MGTHRXN0	M1	AD6_SERD0_N	AD14_SERD0_N
	MGTHRXP0	M2	AD6_SERD0_P	AD14_SERD0_P
	MGTHRXN1	K1	AD6_SERD1_N	AD14_SERD1_N
	MGTHRXP1	K2	AD6_SERD1_P	AD14_SERD1_P
	MGTHRXN2	H1	AD7_SERD0_N	AD15_SERD0_N
	MGTHRXP2	H2	AD7_SERD0_P	AD15_SERD0_P
	MGTHRXN3	F1	AD7_SERD1_N	AD15_SERD1_N
	MGTHRXP3	F2	AD7_SERD1_P	AD15_SERD1_P

Table A1-2: Connessioni JESD ADC-FPGA.

Le line di controllo ADC JESD sono connesse al Banco 65 del corrispondente dispositivo FPGA.
L'alimentazione del banco e' 2,5V.

Banco	Nome Pin	Pin	iTPM signale FPGA 0	iTPM signale FPGA 1
B65	IO_L4N_T0U_N7_DBC_AD7N	AN12	AD0_FD_A	AD8_FD_A
	IO_L3P_T0L_N4_AD15P	AM11	AD0_FD_B	AD8_FD_B
	IO_T0U_N12	AK11	AD1_FD_A	AD9_FD_A
	IO_L22N_T3U_N7_DBC_AD0N	AP8	AD1_FD_B	AD9_FD_B
	IO_T3U_N12	AM9	AD2_FD_A	AD10_FD_A
	IO_L21N_T3L_N5_AD8N	AL9	AD2_FD_B	AD10_FD_B
	IO_L23P_T3U_N8	AJ9	AD3_FD_A	AD11_FD_A
	IO_L11N_T1U_N9_GC	AH12	AD3_FD_B	AD11_FD_B
	IO_L11P_T1U_N8_GC	AG12	AD4_FD_A	AD12_FD_A
	IO_L14N_T2L_N3_GC	AG9	AD4_FD_B	AD12_FD_B
	IO_L15P_T2L_N4_AD11P	AE8	AD5_FD_A	AD13_FD_A
	IO_L15N_T2L_N5_AD11N	AF8	AD5_FD_B	AD13_FD_B
	IO_L16N_T2U_N7_QBC_AD3N	AE10	AD6_FD_A	AD14_FD_A
	IO_L10N_T1U_N7_QBC_AD4N	AE11	AD6_FD_B	AD14_FD_B
	IO_L7P_T1L_N0_QBC_AD13P	AE13	AD7_FD_A	AD15_FD_A
	IO_L9P_T1L_N4_AD12P	AE12	AD7_FD_B	AD15_FD_B
	IO_L13N_T2L_N1_GC_QBC	AG10	CLK_FPGA0_N	CLK_FPGA1_N
	IO_L13P_T2L_N0_GC_QBC	AF10	CLK_FPGA0_P	CLK_FPGA1_P
	IO_L5N_T0U_N9_AD14N	AL12	FPGA0_SYNC_AD0	FPGA1_SYNC_AD8
	IO_L19N_T3L_N1_DBC_AD9N	AM10	FPGA0_SYNC_AD1	FPGA1_SYNC_AD9
	IO_L19P_T3L_N0_DBC_AD9P	AL10	FPGA0_SYNC_AD2	FPGA1_SYNC_AD10
	IO_L24P_T3U_N10	AK8	FPGA0_SYNC_AD3	FPGA1_SYNC_AD11
	IO_L18P_T2U_N10_AD2P	AH9	FPGA0_SYNC_AD4	FPGA1_SYNC_AD12
	IO_L14P_T2L_N2_GC	AF9	FPGA0_SYNC_AD5	FPGA1_SYNC_AD13
	IO_L17P_T2U_N8_AD10P	AD9	FPGA0_SYNC_AD6	FPGA1_SYNC_AD14
	IO_L9N_T1L_N5_AD12N	AF12	FPGA0_SYNC_AD7	FPGA1_SYNC_AD15
	IO_L2P_T0L_N2	AN13	PLL_SYSREF_REQ	U3_SYSREF_REQ
	IO_L6N_T0U_N11_AD6N	AL13	PPS_IN	PPS_IN
	IO_L12N_T1U_N11_GC	AH11	SYSREF_FPGA0_N	SYSREF_FPGA1_N
	IO_L12P_T1U_N10_GC	AG11	SYSREF_FPGA0_P	SYSREF_FPGA1_P
	IO_L1N_T0L_N1_DBC	AP10	U2_SYSREF_N	U3_SYSREF_N
	IO_L1P_T0L_N0_DBC	AP11	U2_SYSREF_P	U3_SYSREF_P

Table A1-3: Connessioni FPGA-ADC.

3. FPGA - 4X10 QSFP+ & 10G ETH CLOCK

Banco	Nome Pin	Pin	iTPM segnale FPGA 0	iTPM segnale FPGA 1
B228	MGTREFCLK0N	K5	CLK_156_N	nc
	MGTREFCLK0P	K6	CLK_156_P	nc
	MGTHRXN1	D1	10GE0_RX1_N	10GE1_RX1_N
	MGTHRXP1	D2	10GE0_RX1_P	10GE1_RX1_P
	MGTHRXN0	E3	10GE0_RX2_N	10GE1_RX2_N
	MGTHRXP0	E4	10GE0_RX2_P	10GE1_RX2_P
	MGTHRXN2	B1	10GE0_RX3_N	10GE1_RX3_N
	MGTHRXP2	B2	10GE0_RX3_P	10GE1_RX3_P
	MGTHRXN3	A3	10GE0_RX4_N	10GE1_RX4_N
	MGTHRXP3	A4	10GE0_RX4_P	10GE1_RX4_P
	MGTHTXN1	D5	10GE0_TX1_N	10GE1_TX1_N
	MGTHTXP1	D6	10GE0_TX1_P	10GE1_TX1_P
	MGTHTXN0	F5	10GE0_TX2_N	10GE1_TX2_N
	MGTHTXP0	F6	10GE0_TX2_P	10GE1_TX2_P
	MGTHTXN2	C3	10GE0_TX3_N	10GE1_TX3_N
	MGTHTXP2	C4	10GE0_TX3_P	10GE1_TX3_P
	MGTHTXN3	B5	10GE0_TX4_N	10GE1_TX4_N
	MGTHTXP3	B6	10GE0_TX4_P	10GE1_TX4_P
	MGTREFCLK1N	H5	10G_CLK0_N	10G_CLK1_N
	MGTREFCLK1P	H6	10G_CLK0_P	10G_CLK1_P

Table A1-4: Connessioni FPGA-QSFP.

4. FPGA - BUS INTERNO

I segnali INTBUS sono sui banchi 67, 68, alimentati con DDR_VDD.

Banco	Nome Pin	Pin	iTPM segnale FPGA 0	iTPM segnale FPGA 1
	IO_L12N_T1U_N11_GC	C24	FPGA_INTBUS_CLK0_N	FPGA_INTBUS_CLK1_N
	IO_L12P_T1U_N10_GC	D24	FPGA_INTBUS_CLK0_P	FPGA_INTBUS_CLK1_P
	IO_L11N_T1U_N9_GC	D25	FPGA_INTBUS_CLK1_N	FPGA_INTBUS_CLK0_N
	IO_L11P_T1U_N8_GC	E25	FPGA_INTBUS_CLK1_P	FPGA_INTBUS_CLK0_P
	IO_L13N_T2L_N1_GC_QBC	G16	FPGA_INTBUS_CLK2_N	FPGA_INTBUS_CLK3_N
	IO_L13P_T2L_N0_GC_QBC	G17	FPGA_INTBUS_CLK2_P	FPGA_INTBUS_CLK3_P
	IO_L12N_T1U_N11_GC	E17	FPGA_INTBUS_CLK3_N	FPGA_INTBUS_CLK2_N
	IO_L12P_T1U_N10_GC	E18	FPGA_INTBUS_CLK3_P	FPGA_INTBUS_CLK2_P
	IO_L23N_T3U_N9	F22	FPGA_INTBUS_CTRL0	FPGA_INTBUS_CTRL1
	IO_L23P_T3U_N8	G22	FPGA_INTBUS_CTRL1	FPGA_INTBUS_CTRL0
	IO_L23P_T3U_N8	K16	FPGA_INTBUS_CTRL2	FPGA_INTBUS_CTRL3
	IO_T3U_N12	L17	FPGA_INTBUS_CTRL3	FPGA_INTBUS_CTRL2
	IO_L1N_T0L_N1_DBC	E27	FPGA_INTBUS_D0_N	FPGA_INTBUS_D1_N
	IO_L1P_T0L_N0_DBC	F27	FPGA_INTBUS_D0_P	FPGA_INTBUS_D1_P
	IO_L2N_T0L_N3	B27	FPGA_INTBUS_D1_N	FPGA_INTBUS_D0_N
	IO_L2P_T0L_N2	C27	FPGA_INTBUS_D1_P	FPGA_INTBUS_D0_P
	IO_L3N_T0L_N5_AD15N	D29	FPGA_INTBUS_D2_N	FPGA_INTBUS_D3_N
	IO_L3P_T0L_N4_AD15P	E28	FPGA_INTBUS_D2_P	FPGA_INTBUS_D3_P
	IO_L4N_T0U_N7_DBC_AD7N	A29	FPGA_INTBUS_D3_N	FPGA_INTBUS_D2_N
	IO_L4P_T0U_N6_DBC_AD7P	B29	FPGA_INTBUS_D3_P	FPGA_INTBUS_D2_P
	IO_L5N_T0U_N9_AD14N	C28	FPGA_INTBUS_D4_N	FPGA_INTBUS_D5_N
	IO_L5P_T0U_N8_AD14P	D28	FPGA_INTBUS_D4_P	FPGA_INTBUS_D5_P
	IO_L6N_T0U_N11_AD6N	A28	FPGA_INTBUS_D5_N	FPGA_INTBUS_D4_N
	IO_L6P_T0U_N10_AD6P	A27	FPGA_INTBUS_D5_P	FPGA_INTBUS_D4_P
	IO_L7N_T1L_N1_QBC_AD13N	D26	FPGA_INTBUS_D6_N	FPGA_INTBUS_D7_N
	IO_L7P_T1L_N0_QBC_AD13P	E26	FPGA_INTBUS_D6_P	FPGA_INTBUS_D7_P
	IO_L8N_T1L_N3_AD5N	A25	FPGA_INTBUS_D7_N	FPGA_INTBUS_D6_N
	IO_L8P_T1L_N2_AD5P	B25	FPGA_INTBUS_D7_P	FPGA_INTBUS_D6_P
	IO_L9N_T1L_N5_AD12N	B26	FPGA_INTBUS_D8_N	FPGA_INTBUS_D9_N
	IO_L9P_T1L_N4_AD12P	C26	FPGA_INTBUS_D8_P	FPGA_INTBUS_D9_P
	IO_L10N_T1U_N7_QBC_AD4N	A24	FPGA_INTBUS_D9_N	FPGA_INTBUS_D8_N
	IO_L10P_T1U_N6_QBC_AD4P	B24	FPGA_INTBUS_D9_P	FPGA_INTBUS_D8_P
	IO_L19N_T3L_N1_DBC_AD9N	F25	FPGA_INTBUS_D10_N	FPGA_INTBUS_D11_N
	IO_L19P_T3L_N0_DBC_AD9P	G24	FPGA_INTBUS_D10_P	FPGA_INTBUS_D11_P
	IO_L21N_T3L_N5_AD8N	F24	FPGA_INTBUS_D11_N	FPGA_INTBUS_D10_N
	IO_L21P_T3L_N4_AD8P	F23	FPGA_INTBUS_D11_P	FPGA_INTBUS_D10_P
	IO_L13N_T2L_N1_GC_QBC	C23	FPGA_INTBUS_D12_N	FPGA_INTBUS_D13_N
	IO_L13P_T2L_N0_GC_QBC	D23	FPGA_INTBUS_D12_P	FPGA_INTBUS_D13_P
	IO_L14N_T2L_N3_GC	E23	FPGA_INTBUS_D13_N	FPGA_INTBUS_D12_N
	IO_L14P_T2L_N2_GC	E22	FPGA_INTBUS_D13_P	FPGA_INTBUS_D12_P
	IO_L16N_T2U_N7_QBC_AD3N	C22	FPGA_INTBUS_D14_N	FPGA_INTBUS_D15_N
	IO_L16P_T2U_N6_QBC_AD3P	C21	FPGA_INTBUS_D14_P	FPGA_INTBUS_D15_P
	IO_L15N_T2L_N5_AD11N	B22	FPGA_INTBUS_D15_N	FPGA_INTBUS_D14_N
	IO_L15P_T2L_N4_AD11P	B21	FPGA_INTBUS_D15_P	FPGA_INTBUS_D14_P
	IO_L1N_T0L_N1_DBC	A14	FPGA_INTBUS_D16_N	FPGA_INTBUS_D17_N
	IO_L1P_T0L_N0_DBC	B14	FPGA_INTBUS_D16_P	FPGA_INTBUS_D17_P
	IO_L7N_T1L_N1_QBC_AD13N	C14	FPGA_INTBUS_D17_N	FPGA_INTBUS_D16_N
	IO_L7P_T1L_N0_QBC_AD13P	D14	FPGA_INTBUS_D17_P	FPGA_INTBUS_D16_P
	IO_L2N_T0L_N3	A18	FPGA_INTBUS_D18_N	FPGA_INTBUS_D19_N
	IO_L2P_T0L_N2	A19	FPGA_INTBUS_D18_P	FPGA_INTBUS_D19_P
	IO_L4N_T0U_N7_DBC_AD7N	B19	FPGA_INTBUS_D19_N	FPGA_INTBUS_D18_N

Banco	Nome Pin	Pin	iTPM segnale FPGA 0	iTPM segnale FPGA 1
	IO_L4P_T0U_N6_DBC_AD7P	C19	FPGA_INTBUS_D19_P	FPGA_INTBUS_D18_P
	IO_L11N_T1U_N9_GC	D16	FPGA_INTBUS_D20_N	FPGA_INTBUS_D21_N
	IO_L11P_T1U_N8_GC	E16	FPGA_INTBUS_D20_P	FPGA_INTBUS_D21_P
	IO_L6N_T0U_N11_AD6N	C17	FPGA_INTBUS_D21_N	FPGA_INTBUS_D20_N
	IO_L6P_T0U_N10_AD6P	C18	FPGA_INTBUS_D21_P	FPGA_INTBUS_D20_P
	IO_L3N_T0L_N5_AD15N	A15	FPGA_INTBUS_D22_N	FPGA_INTBUS_D23_N
	IO_L3P_T0L_N4_AD15P	B15	FPGA_INTBUS_D22_P	FPGA_INTBUS_D23_P
	IO_L8N_T1L_N3_AD5N	D15	FPGA_INTBUS_D23_N	FPGA_INTBUS_D22_N
	IO_L8P_T1L_N2_AD5P	E15	FPGA_INTBUS_D23_P	FPGA_INTBUS_D22_P
	IO_L9N_T1L_N5_AD12N	F14	FPGA_INTBUS_D24_N	FPGA_INTBUS_D25_N
	IO_L9P_T1L_N4_AD12P	F15	FPGA_INTBUS_D24_P	FPGA_INTBUS_D25_P
	IO_L15N_T2L_N5_AD11N	G14	FPGA_INTBUS_D25_N	FPGA_INTBUS_D24_N
	IO_L15P_T2L_N4_AD11P	G15	FPGA_INTBUS_D25_P	FPGA_INTBUS_D24_P
	IO_L17N_T2U_N9_AD10N	H16	FPGA_INTBUS_D26_N	FPGA_INTBUS_D27_N
	IO_L17P_T2U_N8_AD10P	H17	FPGA_INTBUS_D26_P	FPGA_INTBUS_D27_P
	IO_L5N_T0U_N9_AD14N	B16	FPGA_INTBUS_D27_N	FPGA_INTBUS_D26_N
	IO_L5P_T0U_N8_AD14P	B17	FPGA_INTBUS_D27_P	FPGA_INTBUS_D26_P
	IO_L10N_T1U_N7_QBC_AD4N	D18	FPGA_INTBUS_D28_N	FPGA_INTBUS_D29_N
	IO_L10P_T1U_N6_QBC_AD4P	D19	FPGA_INTBUS_D28_P	FPGA_INTBUS_D29_P
	IO_L16N_T2U_N7_QBC_AD3N	F19	FPGA_INTBUS_D29_N	FPGA_INTBUS_D28_N
	IO_L16P_T2U_N6_QBC_AD3P	G19	FPGA_INTBUS_D29_P	FPGA_INTBUS_D28_P
	IO_L18N_T2U_N11_AD2N	H18	FPGA_INTBUS_D30_N	FPGA_INTBUS_D31_N
	IO_L18P_T2U_N10_AD2P	H19	FPGA_INTBUS_D30_P	FPGA_INTBUS_D31_P
	IO_L14N_T2L_N3_GC	F17	FPGA_INTBUS_D31_N	FPGA_INTBUS_D30_N
	IO_L14P_T2L_N2_GC	F18	FPGA_INTBUS_D31_P	FPGA_INTBUS_D30_P
	IO_L17N_T2U_N9_AD10N	A20	FPGA_INTBUS_STROBE0_N	FPGA_INTBUS_STROBE1_N
	IO_L17P_T2U_N8_AD10P	B20	FPGA_INTBUS_STROBE0_P	FPGA_INTBUS_STROBE1_P
	IO_L18N_T2U_N11_AD2N	D21	FPGA_INTBUS_STROBE1_N	FPGA_INTBUS_STROBE0_N
	IO_L18P_T2U_N10_AD2P	D20	FPGA_INTBUS_STROBE1_P	FPGA_INTBUS_STROBE0_P
	IO_L19N_T3L_N1_DBC_AD9N	J14	FPGA_INTBUS_STROBE2_N	FPGA_INTBUS_STROBE3_N
	IO_L19P_T3L_N0_DBC_AD9P	J15	FPGA_INTBUS_STROBE2_P	FPGA_INTBUS_STROBE3_P
	IO_L20N_T3L_N3_AD1N	K17	FPGA_INTBUS_STROBE3_N	FPGA_INTBUS_STROBE2_N
	IO_L20P_T3L_N2_AD1P	K18	FPGA_INTBUS_STROBE3_P	FPGA_INTBUS_STROBE2_P
	IO_T0U_N12_VRP	C29	pull down 240 ohm	pull down 240 ohm
	IO_T0U_N12_VRP	A17	pull down 240 ohm	pull down 240 ohm
	VREF	J20	pull down 500 ohm	pull down 500 ohm
	VREF	L14	pull down 500 ohm	pull down 500 ohm

Table A1-5: Connessioni Bus Interno.